Low Power Circuits with Small Voltage Swing Transmission, Voltage Regeneration, and Wide Bandwidth Architecture

APPENDIX

Eleven figures are attached as appendix pages A2 to A12, shematically showing examples of embodiments of the invention.

Small Swing Signal DRAM Architecture

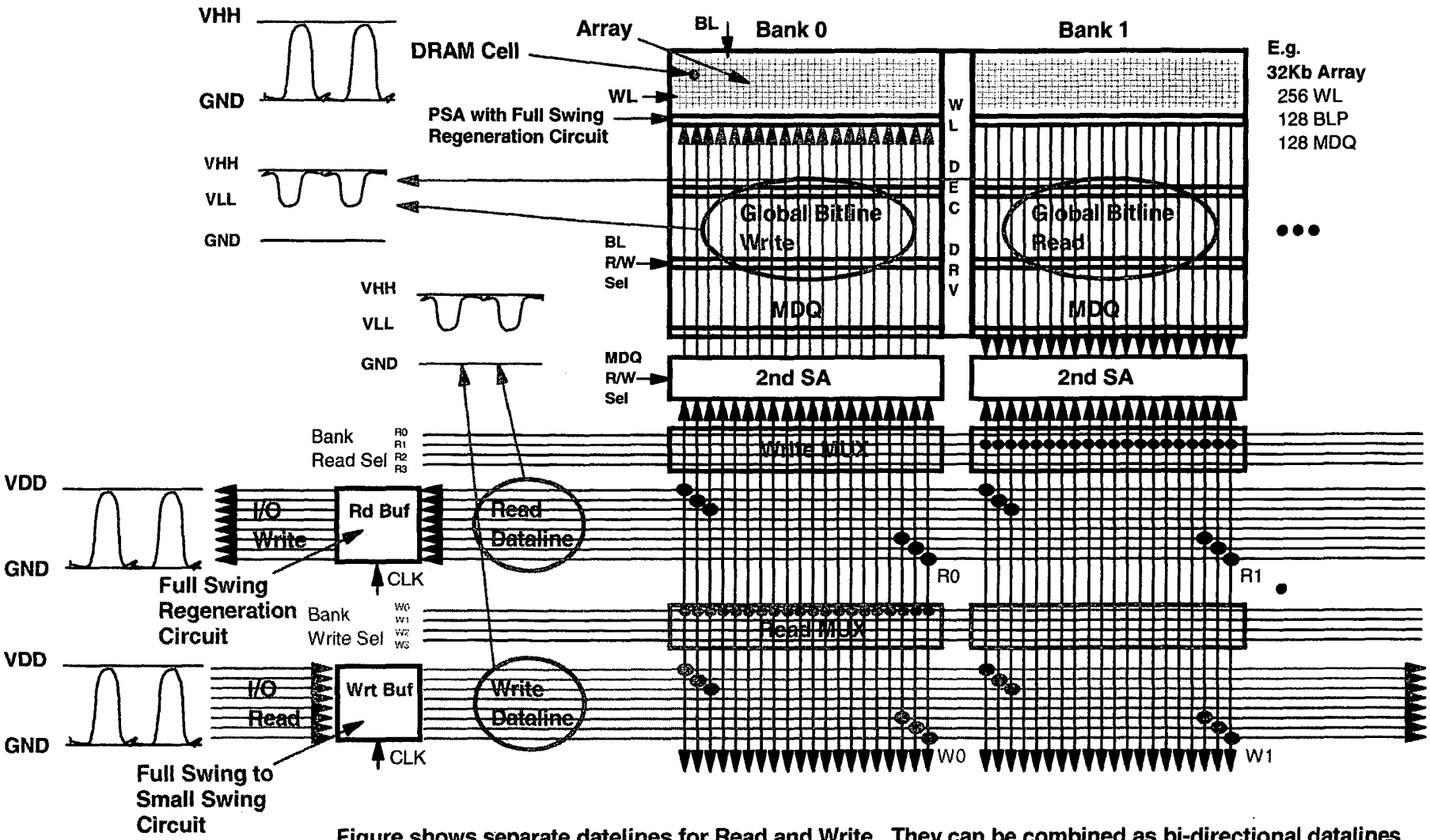
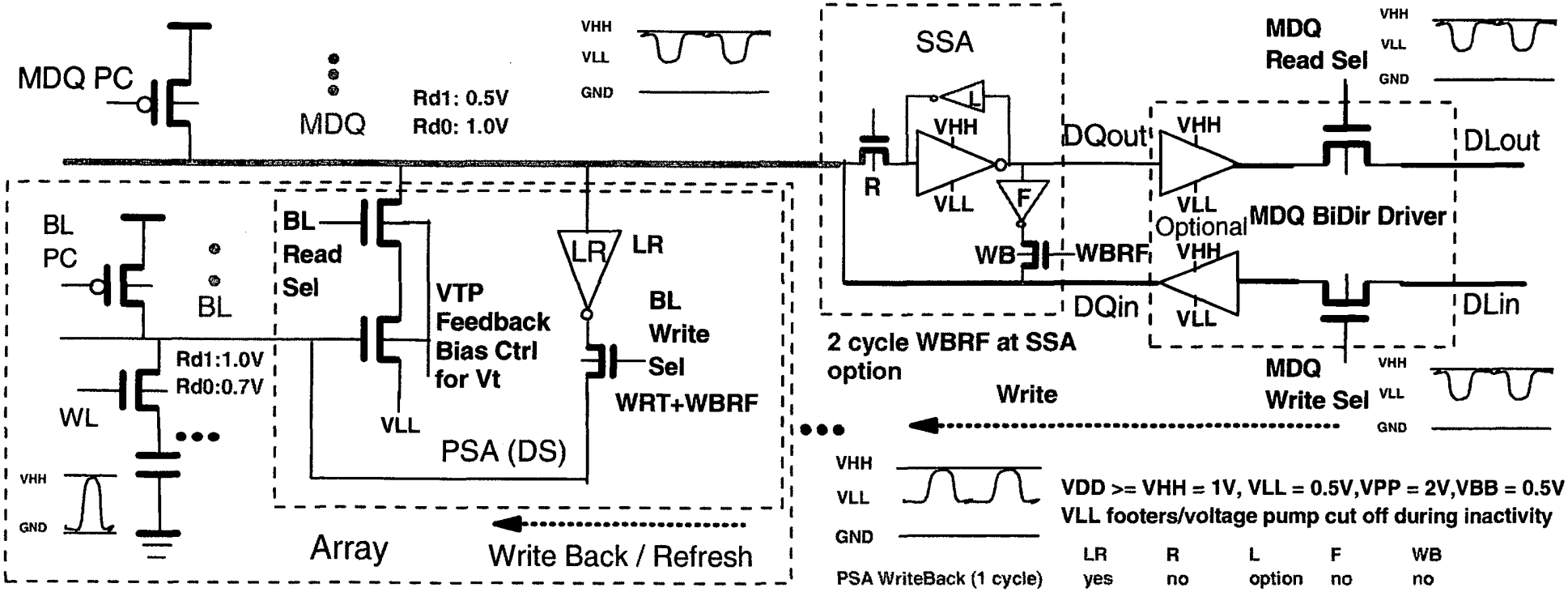


Figure shows separate datelines for Read and Write. They can be combined as bi-directional datalines for both Read and Write.

A2

Low Power Hierarchical Direct Sensing w/ Local Write Back



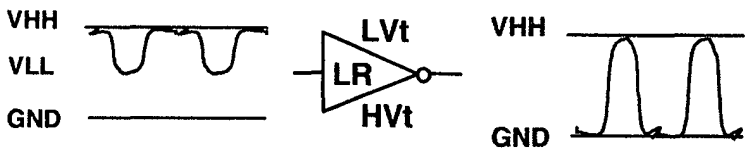
VDD >= VHH = 1V, VLL = 0.5V,VPP = 2V,VBB = 0.5V

VLL footers/voltage pump cut off during inactivity

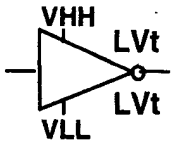
	LR	R	L	F	WB
PSA WriteBack (1 cycle)	yes	no	option	no	no
SSA WriteBack (2 cycle)	yes	yes	yes	yes	yes
SSA WriteBack FS (2 cycle)	no	yes	yes	yes FS	yes
RD	1		1	0	0
WRT	0		0	1	0
MDQ Read Sel	0		1	0	0
MDQ Write Sel	0		0	1	0
WBRF	1		0	0	0
Status	WrtBk / Refrh		Read	Write	Bank off

Read cycle, Write cycle = 3 ns

Read + Write Back cycle = 4.5 ns < Read cycle + Write cycle (6 ns)



P LVt and N HVt devices well bias generated via VTP feedback



N, P LVt devices well bias generat d via VTP feedback

A3

1. Writ Back can b local at PSA or at rem t SSA
2. Write Data can b small wing or full wing on MDQ
3. Local WriteBack (small r power), remote WriteBack (smaller area)
4. Local Writ Back writ s b tter to c lls
5. On cycle or two cycle writeback option

Read, Write, WriteBack Control Table

	LR	R	L	F	WB
PSA WriteBack (1 cycle)	**yes**	**no**	**option**	**no**	**no**
SSA WriteBack (2 cycle)	**yes**	**yes**	**yes**	**yes**	**yes**
SSA WriteBack FS (2 cycle)	**no**	**yes**	**yes**	**yes FS**	**yes**

RD	1	1	0	0
WRT	0	0	1	0
MDQ Read Sel	0	1	0	0
MDQ Write Sel	0	0	1	0
WBRF	1	0	0	0
Status	WrtBk / Refrh	Read	Write	Bank off

1. WriteBack can be local at PSA or at remote SSA

2. Write Data can be small swing or full swing on MDQ

3. Local WriteBack (smaller power), remote WriteBack (smaller area)

4. Local WriteBack writes better to cells

5. One cycle or two cycle writeback option

Read cycle, Write cycle = 3 ns

Read + Write Back cycle = 4.5 ns < Read cycle + Write cycle (6 ns)

The above is the control table for the various operations: READ, WRITE, WRITEBACK REFRESH. For READ operation, RD and MDQ_READ_SEL are HIGH. For WRITE operation, WRT and MDQ_WRITE_SEL are HIGH. For WRITEBACK REFRESH operation, RD and WRBF are HIGH.

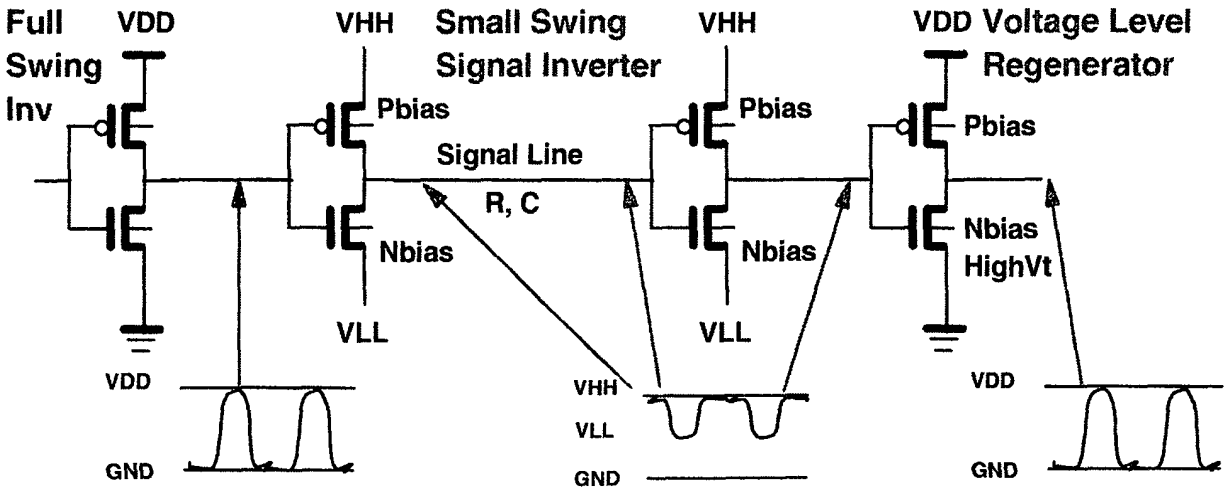
Since DRAM cell voltage is "destroyed" after each READ operation (due to charge sharing), WRITEBACK is an operation to restore the DRAM cell voltage (logic data) after a READ.

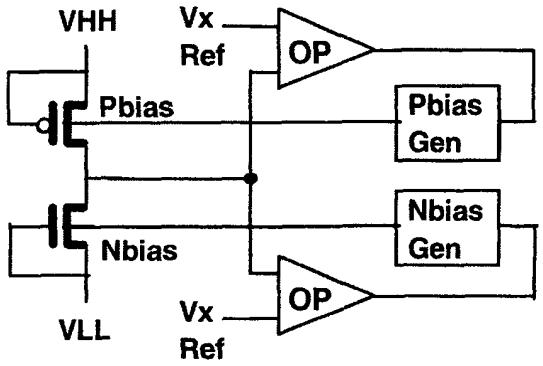
For PSA (primary sense amplifer) to perform a WRITEBACK, the level restoring logic LR is used, as shown in the above table.

WRITEBACK can be performed from the SSA, by using the level restoring logic LR, the READ mux (R), the SSA latch (L), the SSA feedback logic (F) and the SSA WRIETBACK mux (WB), as shown in the above table.

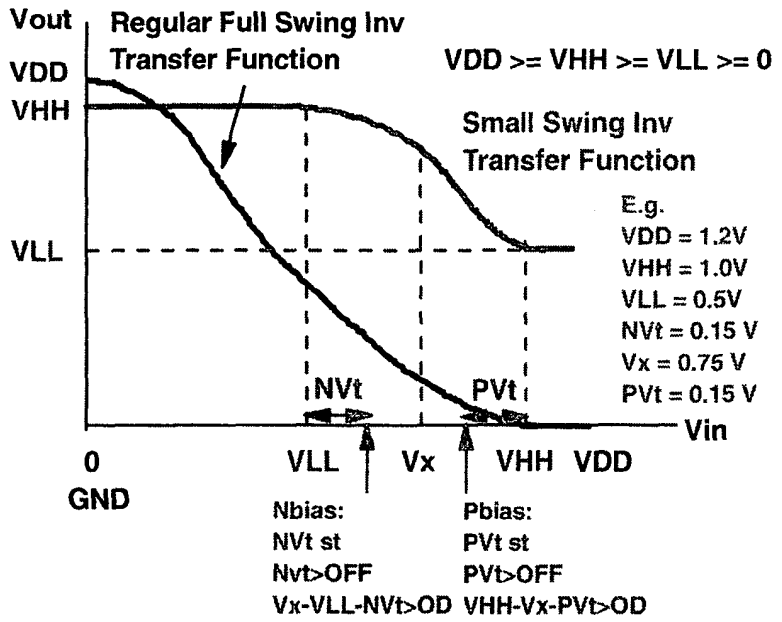
The tradional full swing WRITEBACK can be performed from the SSA, without the level restoring logic (LR) in the PSA, the READ mux (R), the SSA latch (L), the SSA feedback logic (F) operated in full swing mode, and the SSA WRITEBACK mux (WB), as shown in the above table.

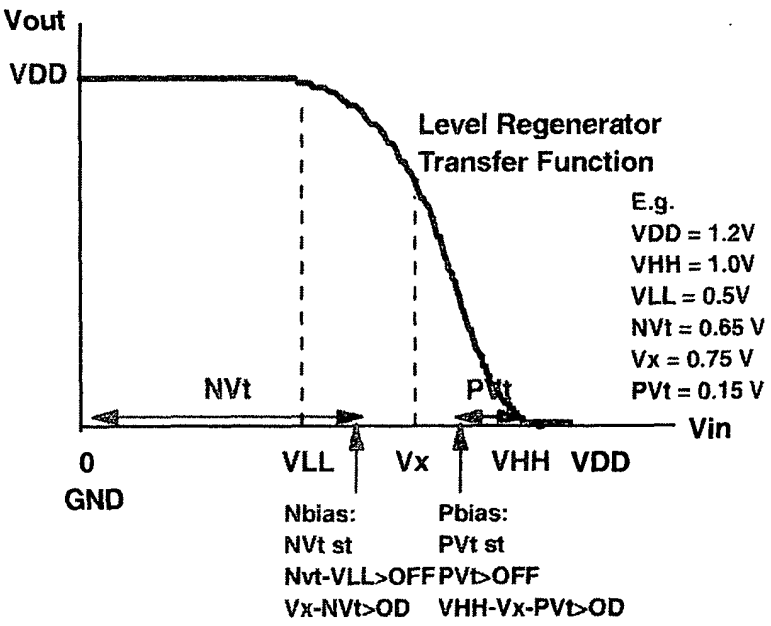
Small Swing Signal Inverter, Level Regenerator and Bias Generator





N, P device well bias generators
(applicable to both SWS Inv and VLR)

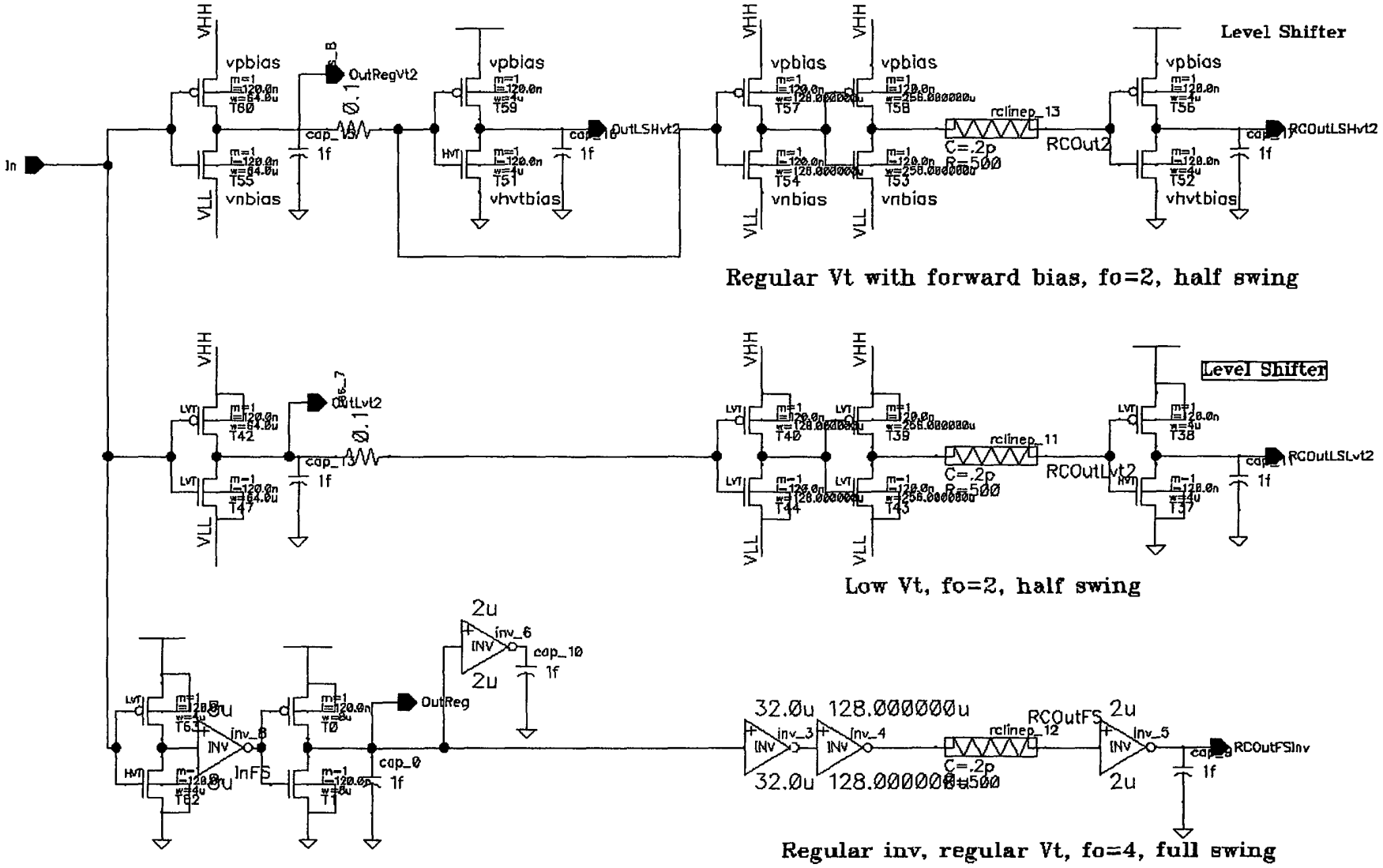




N, P d vic well bias of Small Swing Inv is gen rated via VTP feedback

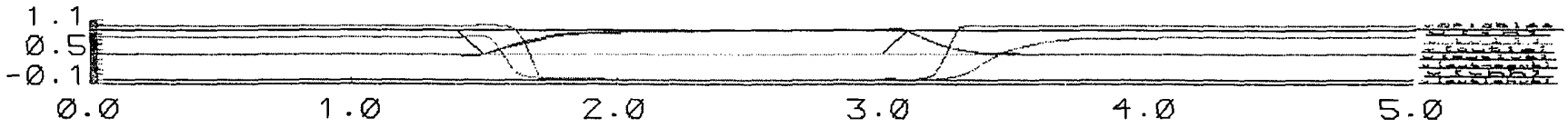
N, P devic w ll bias of L v l R gen rator is g n rated via VTP feedback

Small Voltage Swing Data Transmission and Regeneration

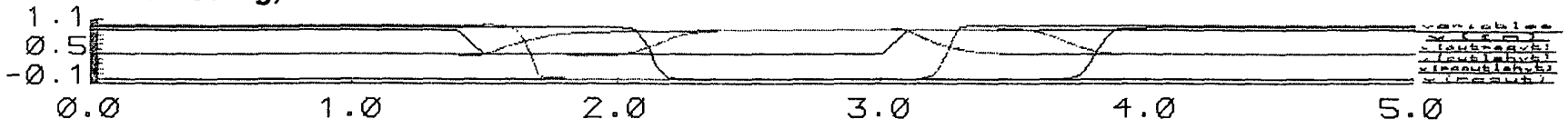


*BIN: ----

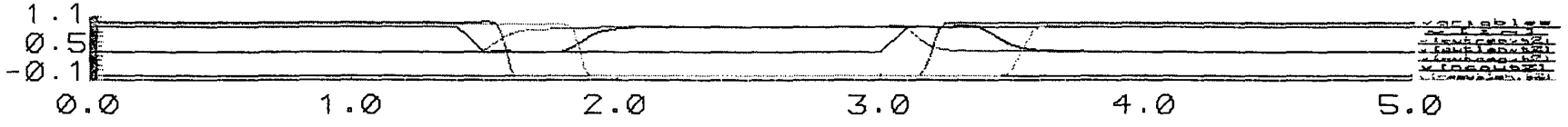
Small Voltage Swing Data Transmission and Regeneration



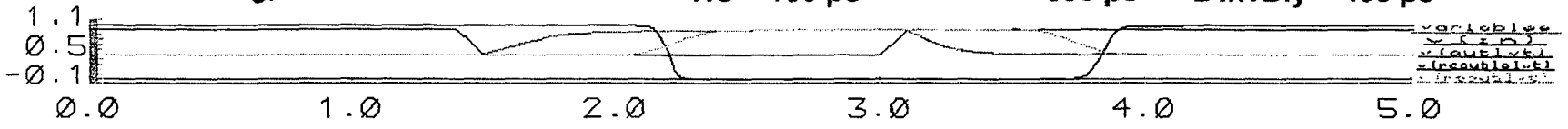
Half Swing, LVT FO=4



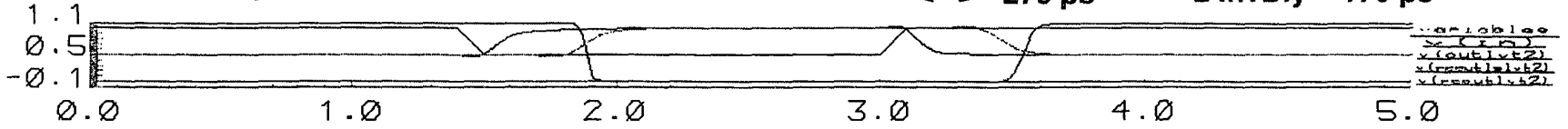
Half Swing, LVT FO=2



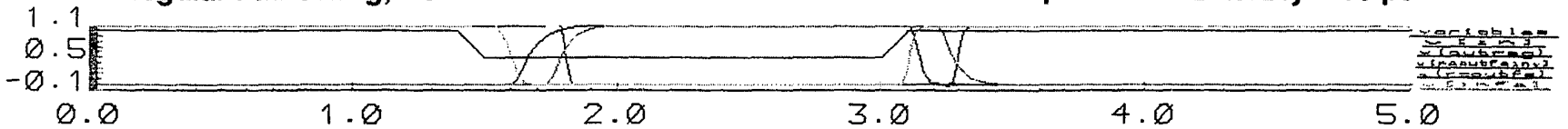
Half Swing, Well Bias FO=4 RC = 100 ps ⟷ 500 ps 2 InvDly = 400 ps



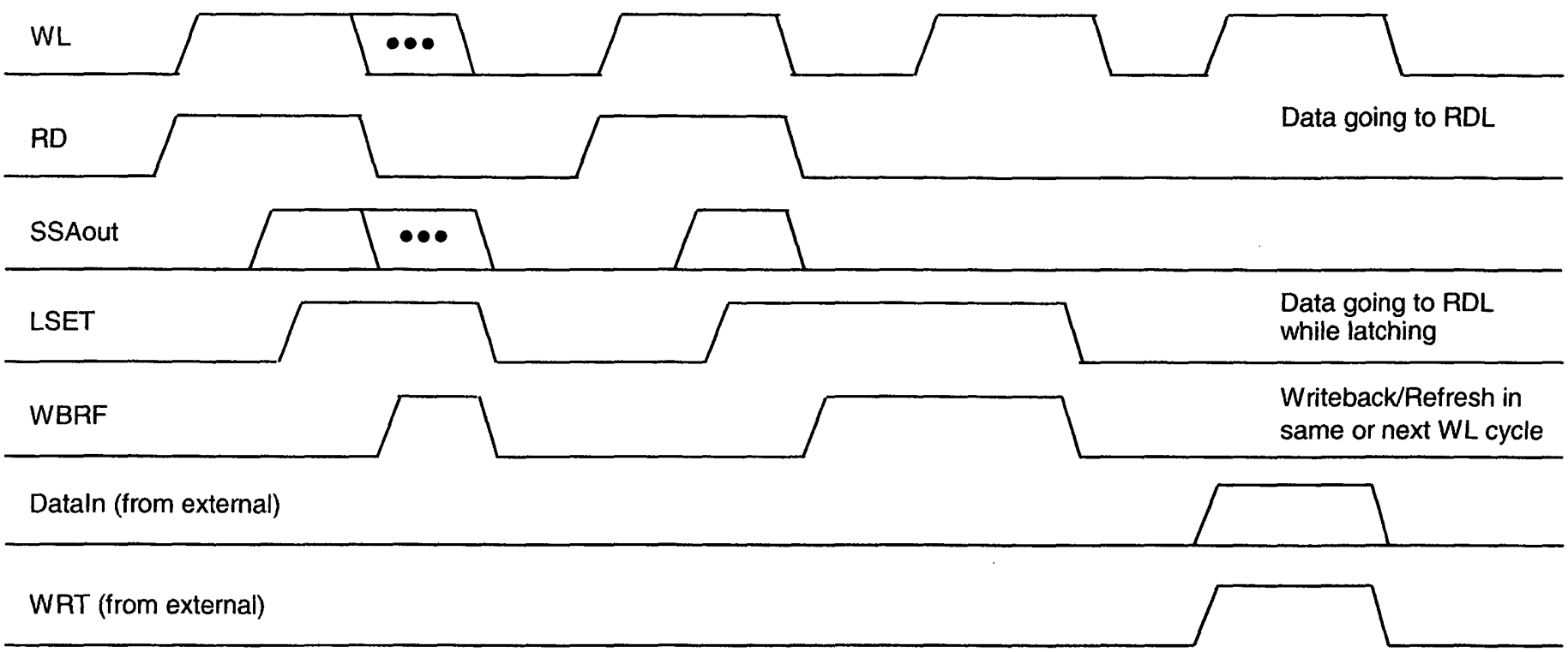
Half Swing, Well Bias FO=2 ⟷ 270 ps 2 InvDly = 170 ps



Regular Full Swing, FO=4 ⟷ 180 ps 2 InvDly = 80 ps



Different Mode of Read, Write and WriteBack/Refresh

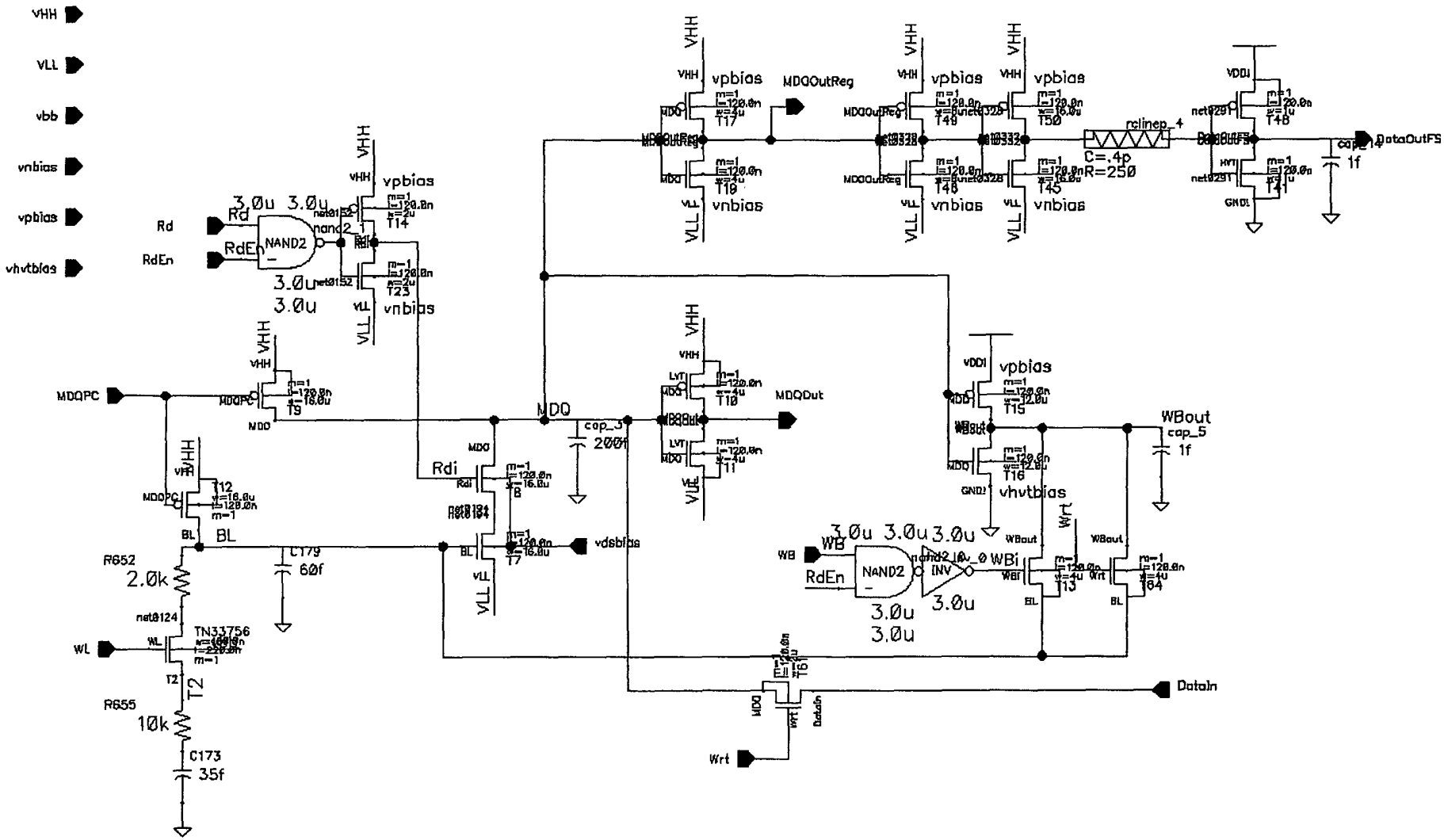


Read and WriteBack
in same WL Cycle (4.5 ns)
Same for Refresh

Read and WriteBack (Refresh)
in two WL Cycles (3.3 ns each)
Same for Refresh

Write in one
WL Cycle (3.3 ns)

Small Voltage Swing Hierarchical Direct Sensing (with Local WriteBack, Small Swing Write Data)



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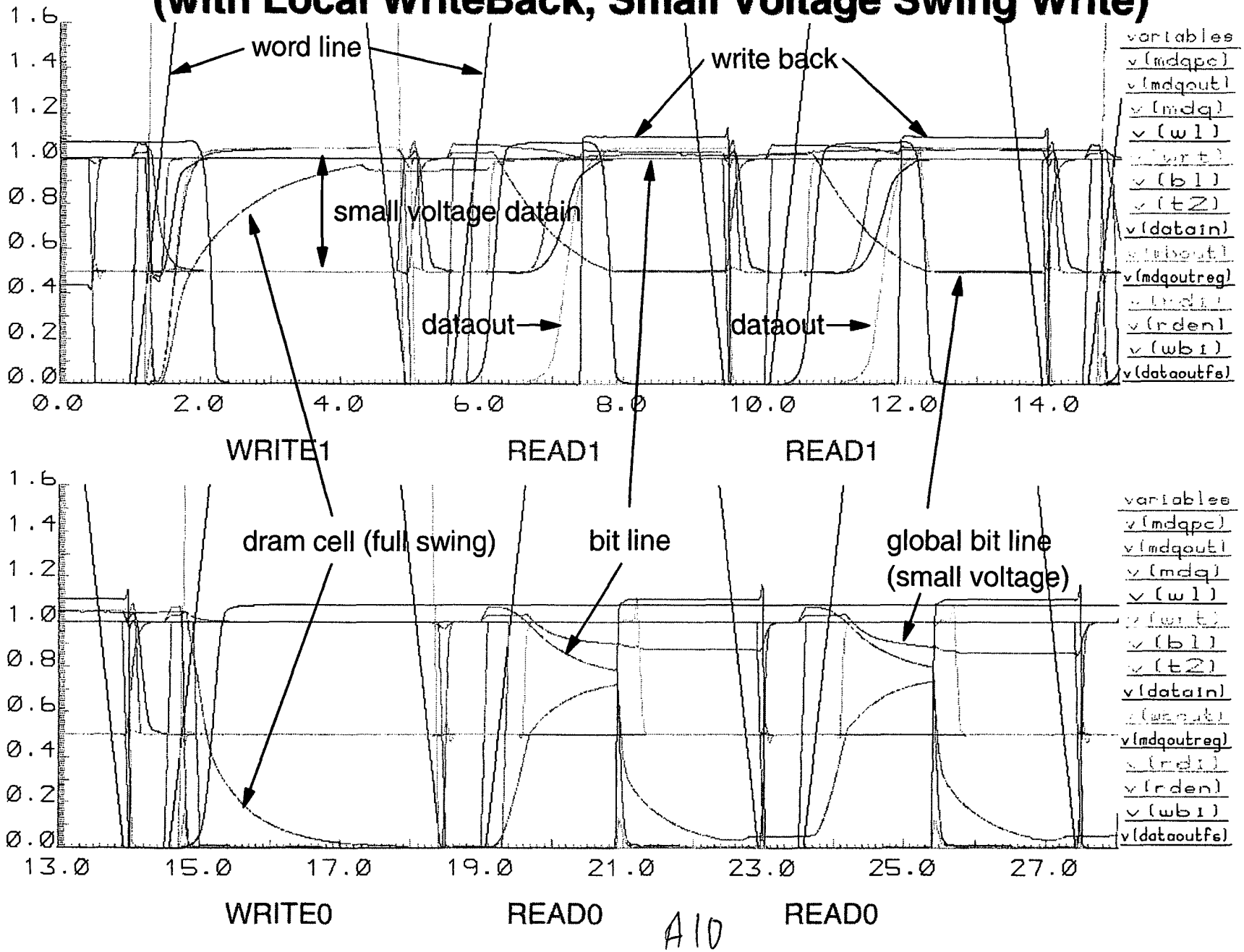
Small Voltage Swing Hierarchical Direct Sensing (with Local WriteBack, Small Voltage Swing Write)



A10

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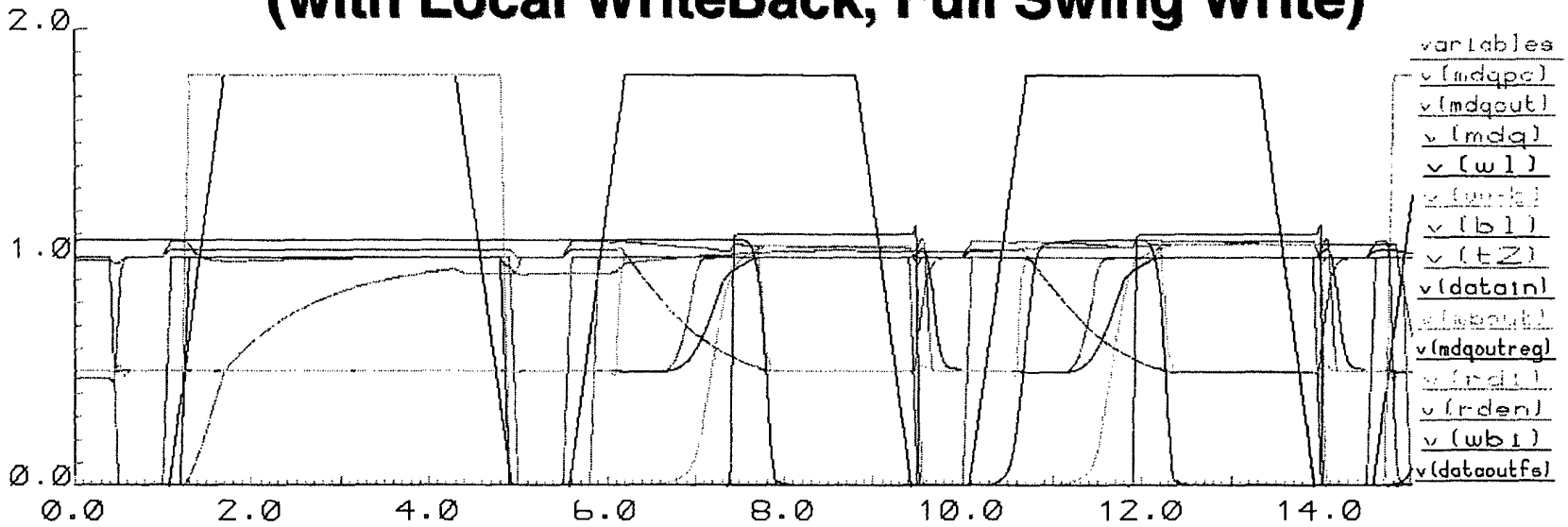
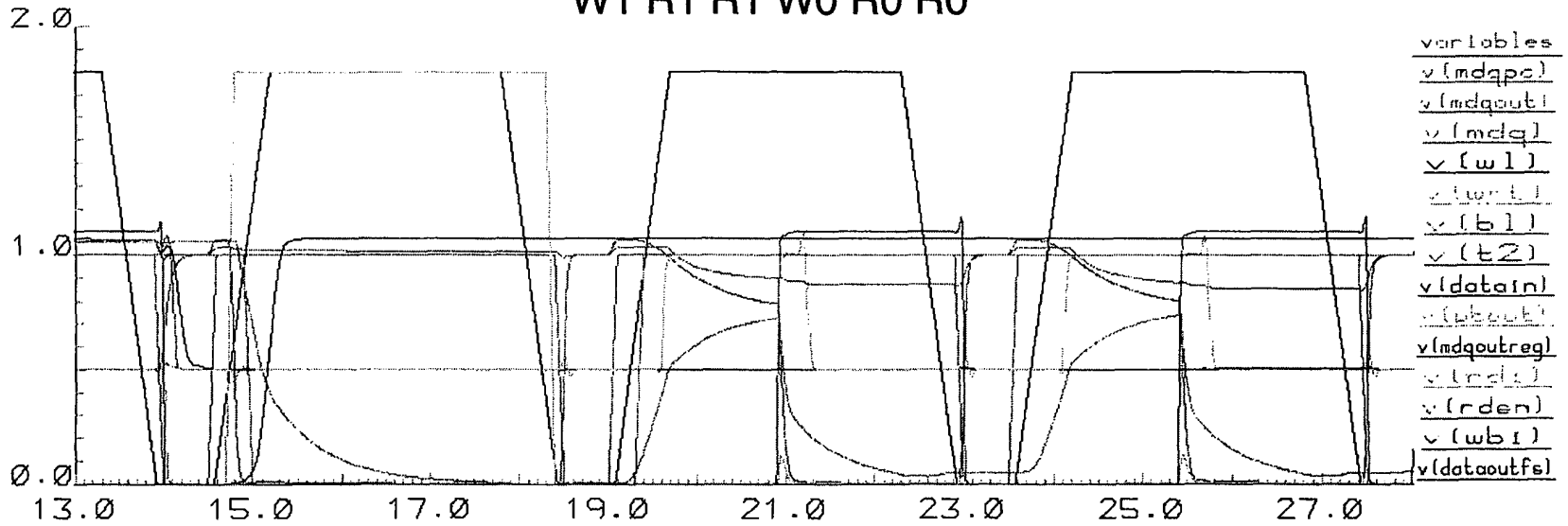
Small Voltage Swing Hierarchical Direct Sensing (with Local WriteBack, Full Swing Write)



W1 R1 R1 W0 R0 R0



A 11

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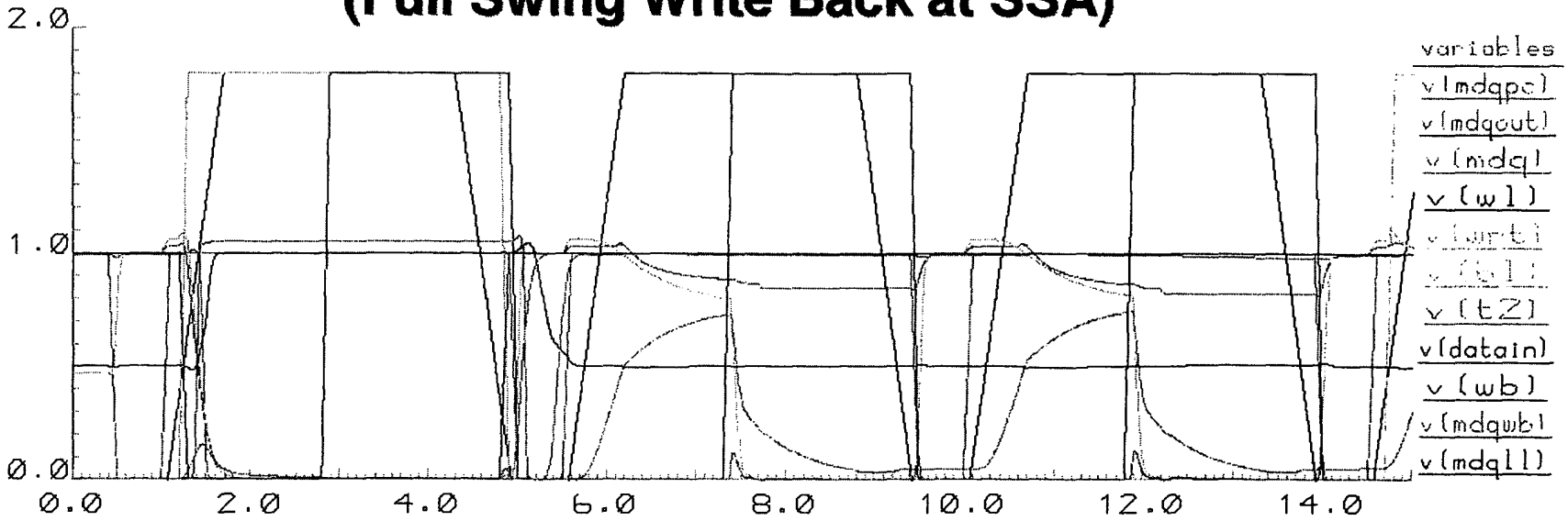
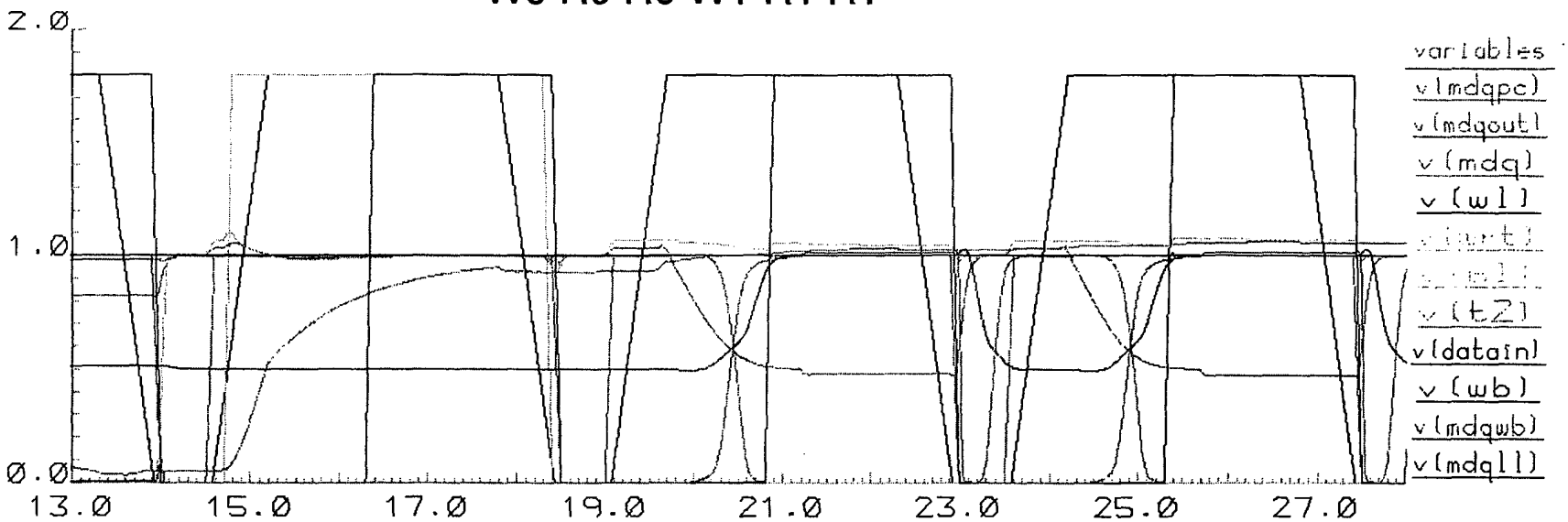
Small Voltage Swing Hierarchical Direct Sensing (Full Swing Write Back at SSA)



W0 R0 R0 W1 R1 R1



A 12